Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **A1**
2. **B1**
3. **Y1**
4. **A2**
5. **B2**
6. **Y2**
7. **GND**
8. **Y3**
9. **A3**
10. **B3**
11. **Y4**
12. **A4**
13. **B4**
14. **VCC**

**9 10 11 12 13**

**1**

**14**

**6 5 4 3 2**

**7**

**8**

**.044”**

**.046”**

**74F00**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: 74F00**

**APPROVED BY: DK DIE SIZE .044” X .046” DATE: 11/14/16**

**MFG: MOTOROLA THICKNESS .015” P/N: 54F00**

**DG 10.1.2**

#### Rev B, 7/19/02